Remarks

This is in response to the Office Action mailed on August 1, 2002. Claims 20 and 44 have been amended, and new claims 49-66 have been added. All amendments and new claims are fully supported by the specification and drawings, and no new matter has been added. Claims 20-24 and 44-66 remain pending in the application. Reconsideration and allowance of all claims are respectfully requested.

Claims 20-24 and 44-48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art, Figures 16 and 17 of the present application (hereinafter the "APA"), in view of Gray, U.S. Patent No. 5,793,126. This rejection is respectfully traversed.

Claim 20 is directed to a semiconductor device having a semiconductor integrated circuit. The device recited by claim 20 includes, inter alia, a first external line provided outside the semiconductor integrated circuit and a first internal terminal provided within the semiconductor integrated circuit. Claim 20 further recites a second connection for connecting the first external line and the second internal terminal. A semiconductor device configured as recited in claim 20 is advantageous for inspecting power source and grounding terminals for a semiconductor integrated circuit.

NP in claim

The rejection states that the APA, as shown in Figure 16 of the present application, includes a first external line (referenced as the line between 1' and L3), a second external line (referenced as the line between 1' and L1), and a second connection (referenced as W1) for connecting the first external line (the line between 1' and L3) and the second internal terminal (referenced as PD1).

However, the second connection W1 in the APA is not connected with the first external line (the line between 1' and L3). Instead, the second connection W1 in the APA is connected with the second external line (the line between 1' and L1). Therefore, the APA does not disclose a second connection for connecting the first external line and the second internal terminal, as recited by claim 20.

Gray is cited solely for disclosing switches. Assuming for the purposes of this response only that this characterization of Gray is accurate, Gray does not remedy the shortcomings of the APA.

For at least this reason, the combination of the APA and Gray fail to render claim 20, as well as claims 21-24 that depend therefrom, obvious. Reconsideration and allowance of claims 20-24 are respectfully requested.

Claim 44 is directed to a method for inspecting a semiconductor device and recites a semiconductor device configured in a manner similar to that recited in claim 20. Therefore, claim 44, as well as claims 45-48 that depend therefrom, should be allowable for at least the same reasons that claim 20 is allowable. Reconsideration and allowance are respectfully requested.

New claims 49-64 are all dependent upon claims 20 or 44, and new claims 65 and 66 are directed to a semiconductor device. All new claims are directed to the elected species or a subspecies of the elected species. Claims 49-66 distinguish over the cited art and should be allowable for at least the same reasons as claims 20 and 44. Consideration and allowance are respectfully solicited.

In view of the above amendments and remarks, all claims are now in condition for allowance. Favorable reconsideration in the form of a Notice of Allowance is respectfully requested. The Examiner is encouraged to contact the undersigned attorney with any questions regarding this application.

Respectfully submitted,

MERCHANT & GOULD P.C.
3200 IDS Center
80 South Eighth Street
Minneapolis, Minnesota 55402
Telephone: (612) 332-5300

Date: December 31, 2002

By: _____
Douglas P. Mueller
Reg. No. 30,300
DPM/RAK

MARKED UP VERSION TO SHOW CHANGES MADE

Please amend claims 20 and 44 as follows.

20. (Once Amended) A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

a first internal line provided within the semiconductor integrated circuit;

a first internal terminal [and], a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit;

a first external line provided outside the semiconductor integrated circuit;

a second external line provided outside the semiconductor integrated circuit and adapted to be connected to the first internal line;

a first connection for connecting the first external line and the first internal terminal;

a second connection for connecting the first external line and the second internal terminal;

a third connection for connecting the second external line and the third internal terminal;

a first switch connected between the first internal terminal and the first internal line; and

a second switch connected between the second internal terminal and the first internal line.

44. (Once Amended) A method for inspecting a semiconductor device comprising: a first internal line provided within the semiconductor integrated circuit; a first internal terminal [and], a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit; a first external line provided outside the semiconductor integrated circuit; a second external line provided outside the semiconductor integrated circuit and adapted to be connected to the first internal line; a first connection for connecting the first external line and the first internal terminal; a second connection for connecting the first external line and the second internal terminal; a third connection for connecting the second external line and the third internal terminal; a first switch connected between the first internal terminal and the first internal line;

and a second switch connected between the second internal terminal and the first internal line, which method comprises:

closing the first switch while opening the second switch;

applying an inspection signal from the first external line to the second external line; and inspecting a connection state between the first external line and the first internal terminal at the first connection.

Please add new claims 49-66 as follows.

49. (New) The semiconductor device according to claim 20, wherein the second external line is connected to the first internal line without passing through a switch.

50. (New) The semiconductor device according to claim 49, wherein the second external line is directly connected to the first internal line.

51. (New) The semiconductor device according to claim 49, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first and second switches.

52. (New) The semiconductor device according to claim 20, further comprising a third switch connected between the third internal terminal and the first internal line.

53. (New) The semiconductor device according to claim 52, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first, second, and third switches.

54. (New) The semiconductor device according to claim 53, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line.

55. (New) The semiconductor device according to claim 53, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit; and

a grounding terminal of the switch controlling section is connected to the third internal terminal.

56. (New) The semiconductor device according to claim 53, wherein:

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit, and

a power source terminal of the switch controlling section is connected to the third internal terminal.

57. (New) The semiconductor device according to claim 52, wherein the third switch is configured to always be on.

58. (New) The semiconductor device according to claim 57, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first, second, and third switches.

59. (New) The semiconductor device according to claim 52, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first and second switches.

60. (New) The method according to claim 44, further comprising a third switch connected between the third internal terminal and the first internal line.

61. (New) The method according to claim 60, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first, second, and third switches.

62. (New) The method according to claim 61, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line.

63. (New) The method according to claim 61, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit; and

a grounding terminal of the switch controlling section is connected to the third internal terminal.

64. (New) The method according to claim 61, wherein:

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit, and

a power source terminal of the switch controlling section is connected to the third internal terminal.

65. (New) A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

an internal line provided within the semiconductor integrated circuit;

a first internal terminal, a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit;

a first connection adapted for connecting an external line and the first internal terminal;

a second connection adapted for connecting an external line and the second internal terminal;

a third connection adapted for connecting an external line and the third internal terminal;

a first switch connected between the first internal terminal and the internal line; and

a second switch connected between the second internal terminal and the internal line.

66. The semiconductor device according to claim 65, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first and second switches.